Claims

What is claimed is:

1. A semiconductor substrate comprising:

an SOI structure including a single-crystal silicon layer for forming a device formed on an insulating layer;

a support substrate of a first conductive-type that is provided beneath the insulating layer; and

a well pattern of one of a first conductive type and a second conductive type that is provided in a predetermined region of the support substrate.

2. A semiconductor substrate according to claim 1, wherein a predetermined electric potential is applied to the well pattern via a connection member that passes through the insulating layer.

3. A semiconductor substrate according to claim 1, wherein the predetermined region where the well pattern is provided includes at least another region where a pad is disposed .

4. A semiconductor substrate comprising:

an SOI structure including a single-crystal silicon layer for forming a device formed on an insulating layer;

a support substrate provided beneath the insulating layer; and

a conductive layer pattern provided in a predetermined region of the support substrate.

5. A semiconductor substrate according to claim 4, wherein a predetermined electric potential is applied to the conductive layer pattern via a connection member that passes through the insulating layer.

6. A semiconductor substrate according to claim 4, wherein the predetermined region where the conductive layer pattern is provided includes at least another region where a pad is disposed .

7. A semiconductor substrate according to claim 4, further comprising a well pattern connected with the conductive layer pattern, in the predetermined region of the support substrate.

8. A method of manufacturing a semiconductor substrate comprising the steps of:

preparing a seed substrate, and epitaxially growing a single-crystal silicon layer for forming a device on the seed substrate;

heat-treating the single-crystal silicon layer to form an insulating layer on the single-crystal silicon layer;

preparing a support substrate of a first conductive type and forming at least a well pattern of one of a first conductive type and a second conductive type in a predetermined region;

bonding the support substrate including the well pattern with the insulating layer formed on the single-crystal silicon layer; and

splitting the seed substrate from the insulating layer such that the single-crystal silicon layer is a main surface of the device.

9. A method of manufacturing a semiconductor substrate comprising the steps of:

preparing a seed substrate, and epitaxially growing a single-crystal silicon layer for forming a device on the seed substrate;

heat-treating the single-crystal silicon to form an insulating layer on the single-crystal silicon layer;

preparing a support substrate;

forming at least a conductive layer pattern in a predetermined region of the support substrate, embedding an insulating layer, and then planarizing the surface of the insulating layer;

bonding the support substrate including the conductive layer pattern with the insulating layer on the single crystal silicon; and

splitting the seed substrate from the insulating layer such that the single-crystal silicon layer is the main surface of the device.

10. A method of manufacturing a semiconductor substrate according to claim 9, further comprising a step of forming a well pattern that connects to the conductive layer pattern on the support substrate.

11. A semiconductor device comprising:

a support substrate of a predetermined conductive type that is provided with a well pattern formed in a predetermined region;

an insulating layer on the support substrate;

a single-crystal silicon layer on the insulating layer;

an element isolation region selectively formed in the single-crystal silicon layer;

an integrated circuit element arranged in the single-crystal silicon layer; and

an electrical connection member that passes from the main surface of the integrated circuit element and to the well pattern through the insulating layer.

12. The semiconductor device of claim 11, wherein the well pattern controls the electric potential relating to the integrated circuit element.

13. The semiconductor device of claim 11, wherein the well pattern is used as at least one of a wiring layer and a component in a passive element.

14. A semiconductor device comprising:

a support substrate including a conductive layer pattern formed in a predetermined region;

an insulating layer on the support substrate;

a single-crystal silicon layer on the insulating layer;

an element isolation region selectively formed in the single-crystal silicon layer;

an integrated circuit element arranged upon the single-crystal silicon layer; and

an electrical connection member that passes from the main surface of the integrated circuit element and to the conductive layer pattern through the insulating layer.

15. The semiconductor device of claim 14, wherein the conductive layer pattern controls the electric potential relating to the integrated circuit element.

16. The semiconductor device of claim 14, wherein the conductive layer pattern is used as at least one of a wiring layer and a component in a passive element.

17. A semiconductor device according to claim 14, further comprising a well pattern connected with the conductive layer pattern, in the predetermined region of the support substrate.